"BSX1" EPROM Update

The Version 4.81 EPROM update comes in two forms. The first is an 8k EPROM that will plug into the original "BSX1" PCB without modification. This version does not allow battery backed up RAM, nor intelligent OA lists or a CWID.

The larger eprom upgrade uses different ROM and RAM adressing from the 8k EPROM version of the code. The code automatically scans memory from location $8000 to $FFFF for RAM and allocates available RAM. This version of code also allows battery backup of the RAM.

If the larger EPROM size upgrade is used, some alterations to the BSX1 PCB are therefore required as follows:

If a 27256 EPROM is used:

1. Cut the tracks going to EPROM pins 20,26 and 27.
2. Connect Z80 pin 3 to EPROM pin 26.
3. Connect Z80 pin 4 to EPROM pin 27.
4. Connect Z80 pin 5 to EPROM pin 20.

If a 27128 EPROM is used:

1. Cut the tracks going to pins EPROM 20 and 26.
2. Connect Z80 pin 3 to EPROM pin 26.
3. Connect Z80 pin 5 to EPROM pin 20.

Next:

5. Cut the tracks going to pin 20 on BOTH the RAM chips.
6. Connect pin 5 of the 74HC42 chip (chip select $8000) to pin 20 of one of the RAM chips.
7. Connect pin 6 of the 74HC42 chip (chip select $A000) to pin 20 of the OTHER RAM chip.

Alternatively, a 32k RAM (43256 or 62256) can replace both 6264 RAMS as follows:

5. Cut all tracks going to RAM socket pins 1 2, 20 & 26 (if they exist).
6. Connect EPROM pin 2 to RAM socket pin 2
7. Connect EPROM pin 26 to RAM socket pin 26.
8. Connect Z80 pin 4 to RAM socket pin 1.
9. Cut all tracks going to pins 12 and 13 of the 74HC04 chip.
10. Connect Z80 pin 5 to 74HC04 pin 13.
11. Connect 74HC04 pin 12 to RAM socket pin 20.

All the above-mentioned changes do not allow for battery backed up RAM. To implement the latter, the chip select line to the ROM(s) needs to be disabled during power up and power down. the simplest reliable circuit to do this is shown in Figure 1. A FET is placed in the chip select line of the RAM(s) and driven by a zener diode circuit attached to the 12V line. When the 12V line rises, the chip select line is not enabled until the 12V line reaches 10V; i.e. the 5V line as stable. Conversely, when the 12 volt line drops, the chip select line is disabled when the 12V line drops below 10V; i.e. before the 5 volt line fails.

Best Wishes!
Peter Meiring, G0BSX/GB7PLY
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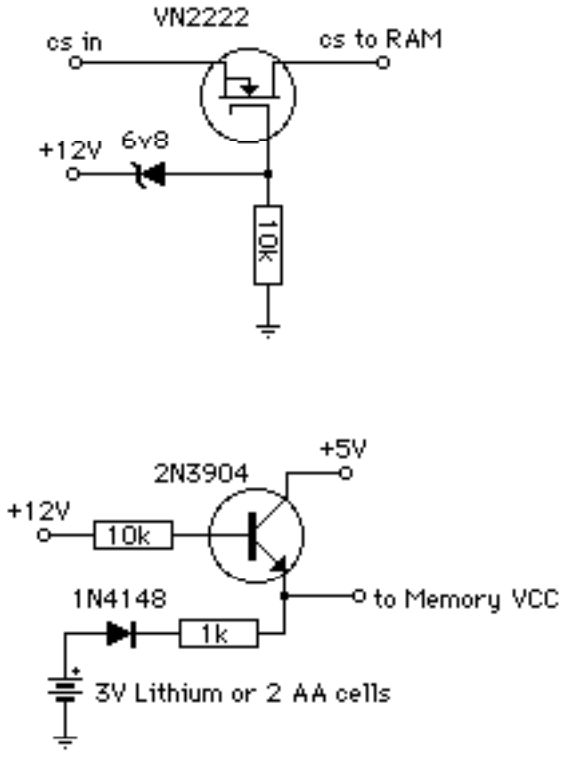

Fig. 1: Chip Select Line